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Description

METHOD FOR PROGRAMMING SINGLE-POLY EPROM AT LOW OPERATION VOLTAGES

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to a method for operating a non-volatile memory cell, and more particularly to a method for programming an electrical programmable read only memory (EPROM) cell at low operation voltages.

[0003] 2. Description of the Prior Art

[0004] Single-poly electrical programmable read only memory (EPROM) devices or one-time programmable (OTP) read only memory devices are known in the art. A single-poly EPROM cell is a non-volatile storage device, which is fabricated using process steps that are fully compatible with conventional single-poly CMOS fabrication process steps. As a result, single-poly EPROM cells are often embedded

in CMOS logic and mixed-signal circuits.

[0005] To save battery power of portable devices, low-voltage operations for EPROM are desired. Prior art such as U.S. Pat. No. 5,761,126 filed February 7, 1997 by Chi et al. entitled "Single-poly EPROM cell that utilizes a reduced programming voltage to program the cell" discloses a single-poly EPROM cell that utilizes a reduced programming voltage to program the cell. The layout and the programming voltage of the single-poly EPROM cell are reduced by eliminating the N^+ contact region which is conventionally utilized to place a positive voltage on the N-well of the cell, and by utilizing a negative voltage of 6V ~ 7V to program the cell. The negative voltage is applied to a P^+ contact region formed in the N-well, which injects electrons directly onto the floating gate of the cell.

[0006] U.S. Pat. No. 6,130,840 filed April 28, 1999 by Bergemont et al. entitled "Memory cell having an erasable Frohmann-Bentchkowsky memory transistor" discloses a memory cell having an erasable Frohmann-Bentchkowsky P-channel memory transistor and an N-channel MOS access transistor. Eraseability is provided by utilizing a P-well which is formed adjacent to the memory transistor, and a floating gate which is formed over both the channel of the mem-

ory transistor and the P-well. With a physical gate length of 0.35 microns based on a 0.35-micron design rule, an operation voltage of 5.75 volts is applied to well and source region of the memory cell.

[0007] U.S. Pat. No. 6,509,606 filed April 1, 1998 by Merrill et al. entitled "Single poly EPROM cell having smaller size and improved data retention compatible with advanced CMOS process" discloses a single-poly EPROM cell that does not incorporate oxide isolation and thereby avoids problems with leakage along the field oxide edge that can lead to degraded data retention. Leakage of a single-poly EPROM cell is prevented by eliminating field oxide isolating the source, channel, and drain from the control gate n-well, and by replacing field oxide surrounding the cell with a heavily doped surface isolation region.

[0008] However, conventional methods for programming the single-poly EPROM are still operated at voltages that are relatively higher than Vcc (input/output supply voltage), for example, a high voltage of about 5~7V that is higher than typical Vcc = 3.3V, thus requiring additional high-voltage circuitry and high-voltage devices thereof. Further, conventional single-poly EPROM technology needs a large cell size and a high voltage to capacitively couple the floating

gate for programming the memory cell.

SUMMARY OF INVENTION

[0009] The primary object of the present invention is to provide a method for efficiently programming a single-poly EPROM cell at ±Vcc (for example: Vcc = 3.3V) voltage conditions.

[0010] According to the claimed invention, a method for programming a single-poly electrical programmable read only memory (EPROM) cell is provided. The single-poly EPROM cell comprises a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device. The P-channel floating gate transistor comprises P^+ drain, P^+ source, P channel defined between the P^+ drain and P^+ source, tunnel oxide on the P channel, and doped ploysilicon floating gate on the tunnel oxide. The N-channel coupling device comprises a polysilicon floating electrode that is electrically connected to the doped ploysilicon floating gate and is capacitively coupled to a control doped region formed in the P-type substrate. The method comprises: grounding the P-type substrate; grounding the N-well; biasing the P^+ drain of the P-channel floating gate transistor to a negative voltage; grounding or floating the P^+ source of the P-channel floating gate transistor; and applying a positive voltage on

the control doped region so that the positive voltage being coupled to the P-doped ploysilicon floating gate. The P channel of the P-channel floating gate transistor is in "OFF" state, and a depletion region and electron-hole pairs are created at a junction between the P^+ drain and the N well, and band-to-band tunneling (BTBT) induced hot electrons will inject into the doped ploysilicon floating gate by tunneling through the tunnel oxide.

[0011] According to one aspect of the present invention, the method comprises: grounding the P-type substrate; grounding the N-well; applying a negative voltage of —Vcc to the P^+ drain of said P-channel floating gate transistor; applying a parasitic BJT turn-on voltage to the P^+ source of the P-channel floating gate transistor; and applying a positive voltage of +Vcc to the control doped region so that the positive voltage of +Vcc being coupled to the doped ploysilicon floating gate.

[0012] Other objects, advantages and novel features of the invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0013] The accompanying drawings are included to provide a

further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0014] Fig.1 shows a plan view of a single-poly EPROM cell according to this invention;

[0015] Fig.2 shows a cross-sectional view of the single-poly EPROM cell taken along line A-A of Fig.1;

[0016] Fig.3 shows a cross-sectional view of the single-poly EPROM cell taken along line B-B of Fig.1;

[0017] Fig.4 shows a cross-sectional view of the single-poly EPROM cell taken along line C-C of Fig.1; and

[0018] Fig.5 and Fig.6 are schematic cross-sectional diagrams showing another preferred embodiment for programming the single-poly EPROM cell of Fig.1 at low voltages, wherein Fig.5 shows a cross-sectional view of the single-poly EPROM cell taken along line B-B of Fig.1; and Fig.6 shows a cross-sectional view of the single-poly EPROM cell taken along line C-C of Fig.1.

DETAILED DESCRIPTION

[0019] The present invention is directed to a feasible method for operating a memory cell, particularly to a single-poly

EPROM cell that is capable of being programmed at high speed and low voltages such as ±Vcc.

[0020] A preferred embodiment in accordance with the present invention will now be explained in detail with reference to the attached schematic diagrams: Fig.1 to Fig.4, wherein Fig.1 shows a plan view of a single-poly EPROM cell 100 according to this invention, Fig.2 shows a cross-sectional view of the single-poly EPROM cell 100 taken along line A-A of Fig.1, Fig.3 shows a cross-sectional view of the single-poly EPROM cell 100 taken along line B-B of Fig.1, while Fig.4 shows a cross-sectional view of the single-poly EPROM cell 100 taken along line C-C of Fig.1.

[0021] First, referring to Fig.1, Fig.2 and Fig.3, the single-poly EPROM cell 100 of this invention comprises a P-channel floating gate transistor 101 comprising spaced-apart P^+ source and P^+ drain regions 124 and 126, which are doped in the N well 120. As best seen in Fig.3, a P channel 129 is defined between the P^+ source region 124 and P^+ drain regions 126. The active area consisting of the P^+ source region 124, P^+ drain regions 126 and the P channel 129 is isolated by field oxide (FOX). It is to be understood that the field oxide may be replaced with other isolation means such as shallow trench isolation (STI) in

other cases. As best seen in Fig.2, in accordance with the preferred embodiment, the N well 120 is formed in a P-type silicon substrate 200. The single-poly EPROM cell 100 further comprises a tunnel oxide film 128 formed on the P channel 129. A doped floating poly gate 122 overlies the tunnel oxide film 128. The P^+ source region 124 and P^+ drain regions 126 are formed at two sides of the doped floating poly gate 122 after the floating poly gate 122 being patterned. According to the preferred embodiment of this invention, the tunnel oxide film 128 has a thickness of about 65 angstroms.

[0022] Referring to Fig.1, Fig.2 and Fig.4, the doped floating poly gate 122 laterally extends to the FOX and is contiguous with a polysilicon floating electrode 132 of a capacitive coupling device 102. According to the preferred embodiment of the present invention, the polysilicon floating electrode 132 is N-type doped poly gate and is patterned simultaneously with the floating poly gate 122. The polysilicon floating electrode 132 covers a portion of the FOX and runs across an N-channel coupling area 130 that is formed in the P-type silicon substrate 200 and is isolated by FOX. As best seen in Fig.2 and Fig.4, a dielectric layer 138 such as silicon dioxide is disposed between the

polysilicon floating electrode 132 and the P-type substrate 200. It is understood that other suitable gate dielectric such as oxynitride may be employed. According to the preferred embodiment, the dielectric layer 138 is 65Å silicon dioxide and is thermally formed simultaneously with the tunnel oxide film 128. N^+ control regions 134 and 136 are formed in the P-type silicon substrate 200 within the N-channel coupling area 130 at both sides of the polysilicon floating electrode 132. The N^+ control regions 134 and 136 are electrically connected to each other by, for example, interconnections. A plurality of contact devices 139 are disposed on the N^+ control regions 134 and 136 for connecting the N^+ control regions 134 and 136 with operation voltage signals. According to the preferred embodiment, an N^- doped region 142 is implanted into the P-type substrate 200 under the polysilicon floating electrode 132. As shown in Fig.1 and Fig.2, the P-type silicon substrate 200 is biased to a substrate voltage V_{sub} through a P^+ pick-up contact region 152.

[0023] One preferred method for programming the single-poly EPROM cell 100 will be explained with reference to Fig.2 to Fig.4. In programming operation, a source voltage V_{SOURCE} is applied to the P^+ source region 124, a drain voltage V_{DRAIN}

is applied to the P^+ drain region 126, a well voltage V_{NW} is applied to the N well 120, and a couple voltage V_{CPUPLE} is applied to the electrically connected N^+ control regions 134 and 136. The P-type silicon substrate 200 is connected to V_{sub}. According to the preferred embodiment, V_{SOURCE} = GROUND or FLOATING, V_{DRAIN} = —Vcc, V_{NW} = GROUND, V_{COUPLE} = Vcc, wherein Vcc is about 3.0V~5V. In a case that Vcc = 3.3V (typical supply voltage for I/O circuit), by way of example, the voltage conditions are: V_{COUPLE} =+3.3V, V_{SOURCE} =0V, V_{DRAIN} =—3.3V, V_{NW} =0V, and V_{sub} =0V.

[0024] Since the N-channel coupling area 130 is much larger than the area of the P-channel floating gate transistor 101, therefore the coupling ratio is approximately equal to 1.0. As a result, the voltage coupled from the N^+ control regions 134 and 136 to the floating polysilicon electrode 132 will be close to 3.3V. Since the floating polysilicon electrode 132 is contiguous with the floating poly gate 122 of the P-channel transistor 101, thus in programming operation, a positive voltage of about 3.3V will be coupled to the floating poly gate 122. Under the above-described voltage conditions, as specifically indicated in Fig.3, the P channel 129 of the transistor 101 is

in "OFF" state, and a depletion region and electron-hole pairs are created at the junction between the P^+ drain 126 and the N well 120, and band-to-band tunneling (BTBT) induced hot electrons will inject into the floating poly gate 122 by tunneling through the tunnel oxide film 128.

[0025] Please refer to Fig.5 and Fig.6. Fig.5 and Fig.6 are schematic cross-sectional diagrams showing another preferred embodiment for programming the single-poly EPROM cell of Fig.1 at low voltages, wherein Fig.5 shows a cross-sectional view of the single-poly EPROM cell taken along line B-B of Fig.1; and Fig.6 shows a cross-sectional view of the single-poly EPROM cell taken along line C-C of Fig.1. In programming operation, likewise, a source voltage V_{SOURCE} is applied to the P^+ source region 124, a drain voltage V_{DRAIN} is applied to the P^+ drain region 126, a well voltage V_{NW} is applied to the N well 120, and a couple voltage V_{CPUPLE} is applied to the electrically connected N^+ control regions 134 and 136. The P-type silicon substrate 200 is connected to V_{sub}. According to this preferred embodiment, $V_{SOURCE} = +V_{BE}$, $V_{DRAIN} = -Vcc$, V_{NW} = GROUND (or $V_{NW} = 0V$), $V_{COUPLE} = Vcc$, wherein Vcc is about 3.0V~5V; V_{BE} is a positive voltage that is larger than 0V. In a case that Vcc = 3.3V (typical supply voltage for I/O cir-

cuit), by way of example, the voltage conditions are: V_{COUPLE} =+3.3V, V_{SOURCE} = 0.7V, V_{DRAIN} =—3.3V, V_{NW} =0V, and V_{sub} =0V.

[0026] Since the N-channel coupling area 130 is much larger than the area of the P-channel floating gate transistor 101, therefore the coupling ratio is approximately equal to 1.0. As a result, the voltage coupled from the N^+ control regions 134 and 136 to the floating polysilicon electrode 132 will be approximately 3.3V. Since the floating polysilicon electrode 132 is contiguous with the floating poly gate 122 of the P-channel transistor 101, thus in programming operation, a positive voltage of about 3.3V will be coupled to the floating poly gate 122. Under the above-described voltage conditions, as specifically indicated in Fig.5, the P channel 129 of the transistor 101 is in "OFF" state, and a depletion region and electron-hole pairs are created at the junction between the P^+ drain 126 and the N well 120, and band-to-band tunneling (BTBT) induced hot electrons will inject into the floating poly gate 122 by tunneling through the tunnel oxide film 128. According to this preferred embodiment, a positive voltage of about +0.7V is applied to P^+ source region 124. The forward bias at the P-N junction (P^+ source region 124

and N well 120) turns on a parasitic bipolar junction transistor (parasitic BJT) 300, wherein the P^+ source region 124 acts as an emitter of the parasitic BJT 300, the P^+ drain region 126 acts as an collector of the parasitic BJT 300, and the N well 120 acts as a base of the parasitic BJT 300. In practice, the magnitude of V_{BE}, which is adequate to turn on the parasitic BJT 300, depends on the P-N junction condition (P^+ source region 124 and N well 120). It is advantageous that when the parasitic BJT 300 is turned on, a large collector-emitter current I_{CE} with abundant electrons flow will supply the electron hole pairs at the drain terminal, thereby enhancing BTBT tunneling, and thus effectively reducing the programming voltage.

[0027] The program disturbance can be inhibited by setting unselected V_{COUPLE} to 0V. In such case, the gate to drain voltage difference will not be high enough to generate band-to-band tunneling induced hot electron injection. Accordingly, select gate (SG) for program voltage inhibition is not necessary.

[0028] Further, in another embodiment, depending on the tunnel oxide thickness and criteria of program speed, the memory cell 100 may be programmed at V_{COUPLE} = Vcc~2Vcc. The memory cell 100 may be erased by ultraviolet irradia-

tion (acts as an OTP cell), while in another case, F-N tunneling electrical erasure may be possible (acts as an EEPROM cell) if giving a high positive voltage on N well 120, drain 126, source 124, and grounding the control regions 134 and 136.

[0029] Those skilled in the art will readily observe that numerous modification and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.